

WHAT IS CLAIMED IS:

- 1 1. A semiconductor chip comprising:
 - 2 a semiconductor substrate comprising an active region;
 - 3 a first structure formed in the active region, the first structure being fully silicided;
 - 4 and
 - 5 at least one dummy silicide structure.
- 1 2. The semiconductor chip of claim 1 wherein the first structure is a transistor gate
2 electrode of a transistor.
- 1 3. The semiconductor chip of claim 2 wherein the transistor further comprises a gate
2 dielectric underlying the first structure, the gate dielectric comprising a high permittivity
3 dielectric selected from the group consisting of aluminum oxide, hafnium oxide, hafnium
4 oxynitride, hafnium silicate, zirconium oxide, zirconium oxynitride, zirconium silicate,
5 yttrium oxide, lanthalam oxide, cerium oxide, titanium oxide, and tantalum oxide.
- 1 4. The semiconductor chip of claim 1 wherein the dummy silicide structure is
2 located in the active region.

- 1 5. The semiconductor chip of claim 1 wherein the dummy silicide structure is
2 located in an isolation region separate from the active region.
- 1 6. The semiconductor chip of claim 1 wherein the first structure and dummy silicide
2 structure each comprises nickel silicide.
- 1 7. The semiconductor chip of claim 1 wherein the first structure and dummy silicide
2 structure each comprises a silicide of a material selected from the group consisting of
3 nickel, cobalt, copper, molybdenum, titanium, tantalum, tungsten, erbium, zirconium, and
4 platinum.
- 1 8. The semiconductor chip of claim 1 wherein the first structure and dummy silicide
2 structure each comprises germanium.
- 1 9. The semiconductor chip of claim 1 wherein the semiconductor substrate is a
2 silicon substrate.
- 1 10. The semiconductor chip of claim 1 wherein the semiconductor substrate is a
2 semiconductor-on-insulator substrate.
- 1 11. The semiconductor chip of claim 1 further comprising a contact etch-stop layer
2 overlying portions of the first structure.

1 12. The semiconductor chip of claim 1 further comprising a dielectric layer overlying
2 the first structure and dummy silicide structure.

1 13. An integrated circuit chip comprising:
2 a substrate having an active region and an isolation region;
3 a transistor formed on the active region, the transistor having a source region, a
4 drain region, and a fully silicided gate electrode; and
5 at least one dummy silicide structure.

1 14. The integrated circuit chip of claim 13 wherein electrical contacts are electrically
2 coupled to the source region, the drain region, and the fully silicided gate electrodes.

1 15. The integrated circuit chip of claim 13 wherein the dummy silicided structure is
2 located in the active region.

1 16. The integrated circuit chip of claim 13 wherein the dummy silicided structure is
2 located in the isolation region.

1 17. The integrated circuit chip of claim 13 wherein the fully silicided gate electrode
2 and dummy silicided structure comprise nickel silicide.

1 18. The integrated circuit chip of claim 13 wherein the fully silicided gate electrode
2 and dummy silicided structure comprise a silicide of a material selected from the group
3 consisting of nickel, cobalt, copper, molybdenum, titanium, tantalum, tungsten, erbium,
4 zirconium, and platinum.

1 19. The integrated circuit chip of claim 13 wherein the fully silicided gate electrode
2 and dummy silicided structure comprise germanium.

1 20. A method of forming a semiconductor device having a fully silicided structure,
2 the method comprising the steps of:

3 providing a substrate having an active region and an isolation region;

4 forming a first polysilicon structure on the substrate;

5 forming a dummy polysilicon structure on the substrate, the dummy polysilicon
6 structure being an inoperative circuit element;

7 forming a metal layer over the first polysilicon structure and the dummy
8 polysilicon structure; and

9 siliciding first polysilicon structure and the dummy polysilicon structure with the
10 metal layer to form a first fully silicided structure and a fully silicided dummy structure.

- 1 21. The method of claim 20 wherein the first polysilicon structure is a gate electrode
2 of a transistor.
- 1 22. The method of claim 20 wherein the first polysilicon structure is located in the
2 active region.
- 1 23. The method of claim 20 wherein the dummy polysilicon structure is located in the
2 inactive region.
- 1 24. The method of claim 20 wherein forming the metal layer includes:
2 forming a dielectric layer over the first polysilicon structure and the dummy
3 polysilicon structure; and
4 planarizing the dielectric layer such that the first polysilicon structure and the
5 dummy polysilicon structure are exposed.
- 1 25. The method of claim 20 wherein the step of siliciding is performed by annealing
2 at a temperature of about 200° C to about 900° C in an ambient comprising nitrogen,
3 helium, argon, or neon.
- 1 26. The method of claim 20 wherein the step of forming the dummy silicided
2 structure is performed by forming the dummy silicided structure in the active region.

- 1 27. The method of claim 20 the step of forming the dummy silicided structure is
2 performed by forming the dummy silicided structure in the isolation region.
- 1 28. The method of claim 20 wherein the first fully silicided structure and the dummy
2 silicided structure comprise nickel silicide.
- 1 29. The method of claim 20 wherein the first fully silicided structure and the dummy
2 silicided structure comprise a silicide of a material selected from the group consisting of
3 nickel, cobalt, copper, molybdenum, titanium, tantalum, tungsten, erbium, zirconium, and
4 platinum.
- 1 30. The method of claim 20 wherein the first fully silicided structure and the dummy
2 silicided structure comprise germanium.
- 1 31. The method of claim 20 wherein the step of forming the first polysilicon structure
2 and the step of forming the dummy polysilicon structure are performed in the same
3 process step.
- 1 32. The method of claim 20 wherein the dummy polysilicon structure is not
2 electrically coupled to an active circuit element.

1 33. The method of claim 20 wherein the first polysilicon structure is a gate of a
2 transistor.

1 34. A method of forming a transistor with fully silicided gate electrode, the method
2 comprising the steps of:

3 providing a substrate having an active region and an isolation region;

4 forming a gate dielectric over the substrate;

5 forming a gate electrode and a dummy electrode over the gate dielectric, the gate
6 electrode and the dummy electrode comprising silicon, the dummy electrode being an
7 inactive circuit element;

8 forming source and drain regions oppositely adjacent the gate electrode to form a
9 transistor;

10 depositing metal over the gate electrode and dummy electrode; and

11 siliciding the gate electrode and the dummy electrode with the metal to form a fully
12 silicided gate electrode and a fully silicided dummy electrode.

1 35. The method of claim 34 wherein the gate electrode is located in the active region.

1 36. The method of claim 34 wherein the dummy electrode is located in the isolation
2 region.

1 37. The method of claim 34 wherein depositing metal includes:
2 forming a dielectric layer over the gate electrode and the dummy electrode; and
3 planarizing the dielectric layer such that the gate electrode and the dummy
4 electrode are exposed.

1 38. The method of claim 34 wherein the step of siliciding is performed by annealing
2 at a temperature of about 200° C to about 900° C in an ambient comprising nitrogen,
3 helium, argon, or neon.

1 39. The method of claim 34 wherein the fully silicided gate electrode and the fully
2 silicided dummy electrode comprise nickel silicide.

1 40. The method of claim 34 wherein the fully silicized gate electrode and the fully
2 silicized dummy electrode comprise a silicide of a material selected from the group
3 consisting of nickel, cobalt, copper, molybdenum, titanium, tantalum, tungsten, erbium,
4 zirconium, and platinum.

1 41. The method of claim 34 wherein the fully silicided gate electrode and the fully
2 silicized dummy electrode comprise germanium.

1 42. The method of claim 34 wherein the step of forming the gate electrode and the
2 dummy electrode are performed in the same process step.

1 43. The method of claim 34 wherein the dummy electrode is not electrically coupled
2 to an active circuit element.